APPLICATION NOTE

Application of the CGY2021G power amplifier

AN97034

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Abstract

The CGY2021G is a monolithic GaAs power amplifier for transmission DCS/PCS applications.
This report contains a description including the power amplifier ,the switching , power control circuits and the operation modes.

APPLICATION NOTE

APPLICATION OF THE CGY2021G POWER AMPLIFIER

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Keywords

Telecom
Demonstration Board
CGY2021G
DCS/PCS
Power control
Power amplifier IC
Transmitter

Date: May 5th, 1997

Summary

This report is intended to provide support for designing power amplifier for DCS/PCS applications.

It contains a description of the power amplifier as well as a brief overview of interstage and input /output matching .

An application example of the CGY2021G is given by means of board description for testing ,recommendations for use ,measurement results ,and performances.

CONTENTS

LIST OF FIGURES

1. INTRODUCTION

This note describes the application of RF monolithic GaAs devices in plastic SMD packages for DCS/PCS power amplifiers.

Their main features are:

-low cost

-100% SMD

-high performance

-low voltage operation

-high efficiency

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/VDD4	6 to8	PA output and supply voltage
GND	9 to 17	ground
DETO	18	detector output
VGG1	19	first and second stages gate bias input voltages
GND	20 to 26	ground
RFI	27	PA input
GND	28	ground
VDD1	29	drain first stage and supply
GND	30	ground
VGG2	31	third and fourth stages gate bias input voltages
GND	32	ground
VDD2	33	drain second stage and supplt
GND	34 to 41	ground
VDD3	42	drain third stage and supply
GND	43 to 48	ground

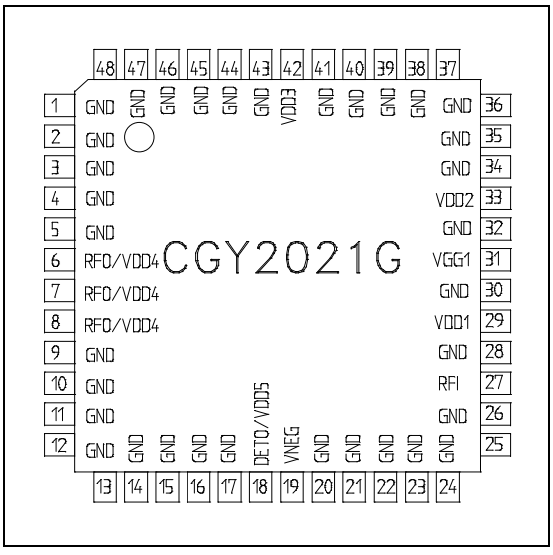

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 Power amplifier

The amplifier is based on a monolithic integrated four stages device using GaAs FET technology in a plastic package.
This device is able to deliver 33 dBm and up to 35 dBm with 4.4 V drain operation.
As described in Fig.2. this device exhibits inter stage matching circuits implemented both on the board and on the chip.Each matching consists of a serie,parallel combination of inductors and capacitors.The serie elements are generally capacitive (MIM capacitors on chip) while the parallel ones can be inductive or capacitive.The parallel matching includes bias pathes and isolation networks for the drains of the different stages.
The input and output matching circuits are implemented on board.
The power amplifier is built on a low cost printed circuit board in association with a switching circuit for pusled applications.This one is able to provide a suitable switching time for DCS and PCS applications.

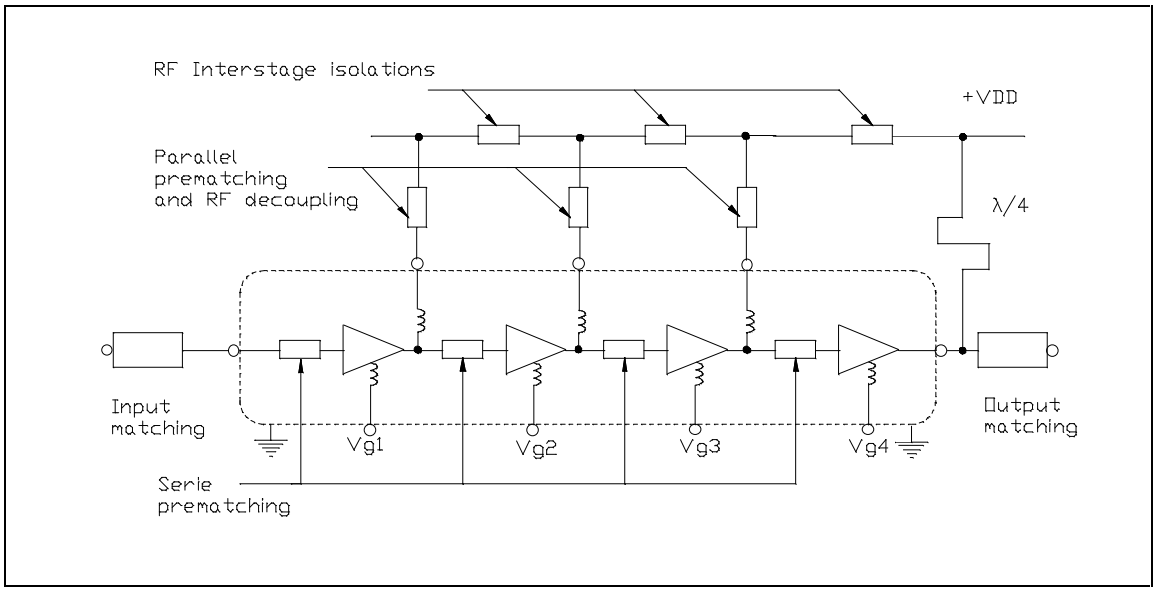

Fig. 2 Power amplifier

3.2 Interstage matchings

The general philosophy used for interstage matching is described when looking at Fig.3.

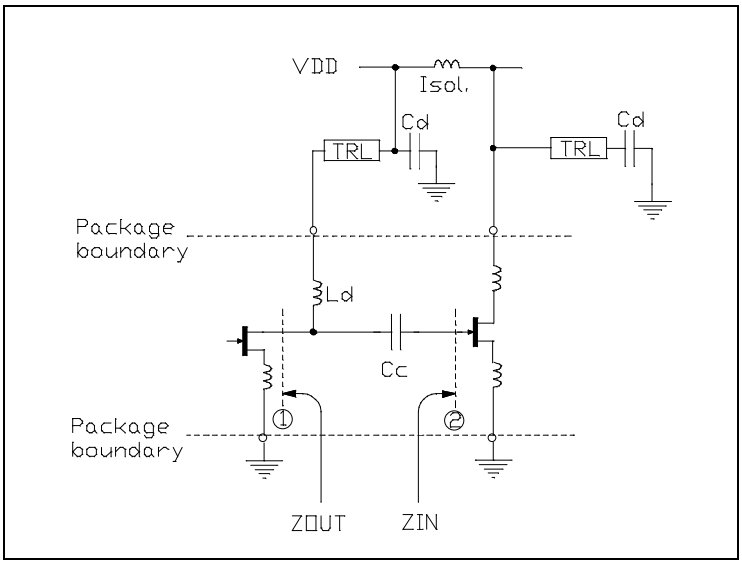

Fig. 3 Interstage matching

The aim is to match the input impedance Zin from a stage in the reference plane 2 to the output impedance Zout of the previous one in the reference plane 1.
This can be accomplished with the interstage coupling capacitor Cc(MIM) on chip ,the bonding wire between the drain and the package lead ,the external transmission line TRL printed on the board and the decoupling capacitor Cd.
As Ld and Cc cannot be adjusted (fixed values),the interstage matching optimisation is carried out by tuning TRL and Cd .

3.3 Drain control and switching circuits

When used in DCS/PCS applications the power amplifier needs to be switched on and off by means of serie element .
For this purpose we use a circuit as described in Fig.4.

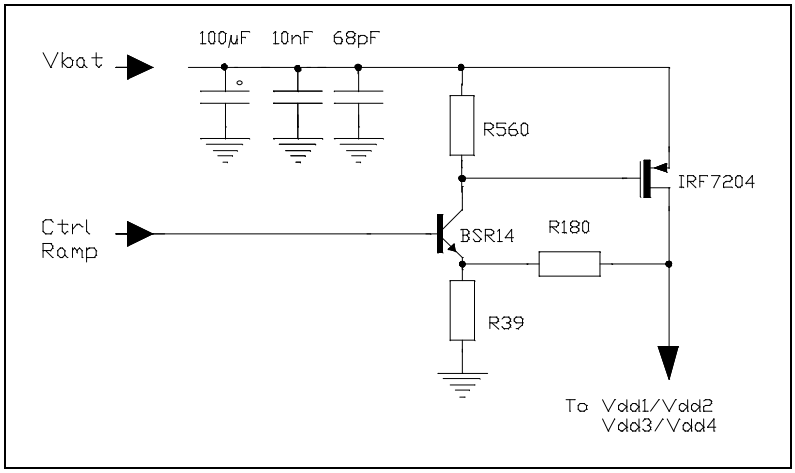

Fig. 4 Drain control and switching circuit

An other way to switch and control the power amplifier is to make use of a specific modulator (UBA1710) intended for these applications with a banbwidth which is around 5 Mhz.
The simplified block diagram is represented in fig .5.
This circuit has the following features :
-Low Rdson N MOS for the switchings
-Voltage tripler for the N MOS control
-Adjustable negative bias for the PA
-Power management disabling the PA when the negative bias is not present
-Stand by gate to switch off the circuit when this one is not in use

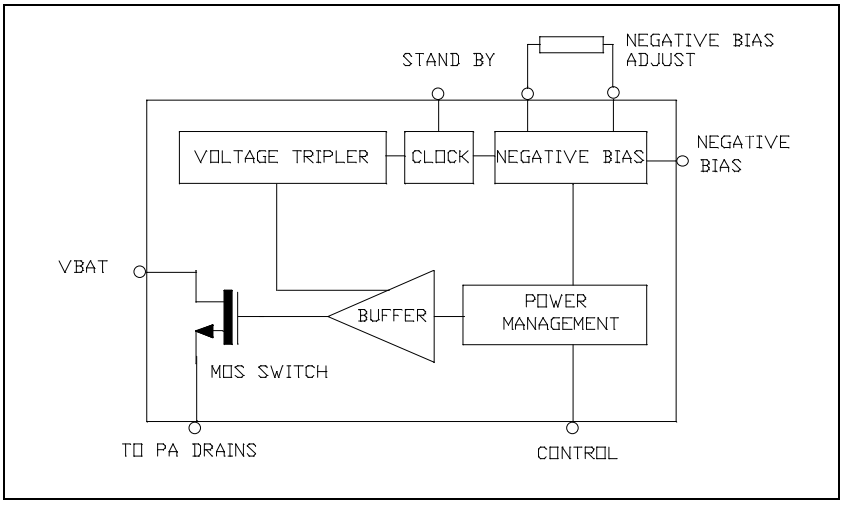

Fig. 5 Modulator

4. MODE OF OPERATION

The device must be operated under pulsed conditions .
The commonly mode of operation in use is class A.
The amplifier must be biased with a negative voltage on the gates in the range of -1V to -2V .
A typical value for the best operation is :-1.6V .
For the drain , the pulsed voltage applied is comprised between 0V and 4.8V ,depending on the powel level we need at the output .
If used with a PMOS as drain control and switch , a negative bias has to be built on the board .
With the use of a UBA1710 modulator , no additionnal negative bias is needed as this one is available in the modulator .
For the RF signal applied to the input port a typical value is 0 dBm continue wave in the DCS/PCS frequency range .

5. GENERAL CHARACTERISTICS

DC CHARACTERISTICS:

VDD=4.5V;Tamb=25°C;peak current values during burst; general operating conditions applied; unless otherwise specified .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Pins RFO/V_{DD4},V_{DD3},V_{DD2},V_{DD1},and DETO/V_{DD5}						
V_{DD}	positive supply voltage		-	4.5	-	V
I_{DD}	positive peak supply current		-	1.4	-	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	-	-1.6	-	V
V_{GG2}	negative supply voltage	note 1	-	-1.6	-	V
I_{GG1} + I_{GG2}	negative peak supply voltage		-	-	2	mA

Note
1- The negative bias V_{GG} must be applied 10µS before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off .

AC-CHARACTERISTICS:

VDD=4.5V; Tamb=25°C; general operating conditions applied; unless otherwise specified .
Measured and guaranteed on CGY2021G evaluation board .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power amplifier						
Pi	input power		-2	-	+2	dBm
S11	input return loss	50 Ω source;note1	-	-	-10	dB

fRF	RF frequency range	DCS	1710	-	1785	MHz
fRF	RF frequency range	PCS	1850	-	1910	MHz
Po(max)	maximum output power	Tamb=25°C; V_{DD}=4.5V	33	34	-	dBm
Po(max)	maximum output power	Tamb=-20 to +85°C;V_{DD}=4.2V	31		-	dBm
η	efficiency	DCS; at Po(max)	40	50	-	%
η	efficiency	PCS; at Po(max)	-	47	-	%
Rs	optimum serie load impedance		-	6	-	Ω
Cs	optimum serie load capacitance		-	11	-	pF
Po(off)	isolation	PA off; Pi=0dBm	-	-50	-	dBm
N_{RX}	output noise in RX band		-	-	-121	dBm/Hz
H2	2nd harmonic level		-	-40	-	dBc
H3	3rd harmonic level		-	-35	-	dBc
Stab	stability	note 2	-	-	-50	dBc
Power sensor driver						
$Po_{(DET)}$			-	-25	-	dBc

Notes

1. Including the 82Ω resistor connected in parallel at the power amplifier input on the evaluation board .
2. The device is adjusted to provide nominal value of load power into a 50 Ω load .The device is switched off and a 6:1 360 electrical degrees during a 60 seconds test period .

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

The circuit diagram used for testing and described in Fig.6 is the one making use of a CGY2021G in association with the UBA1710 .

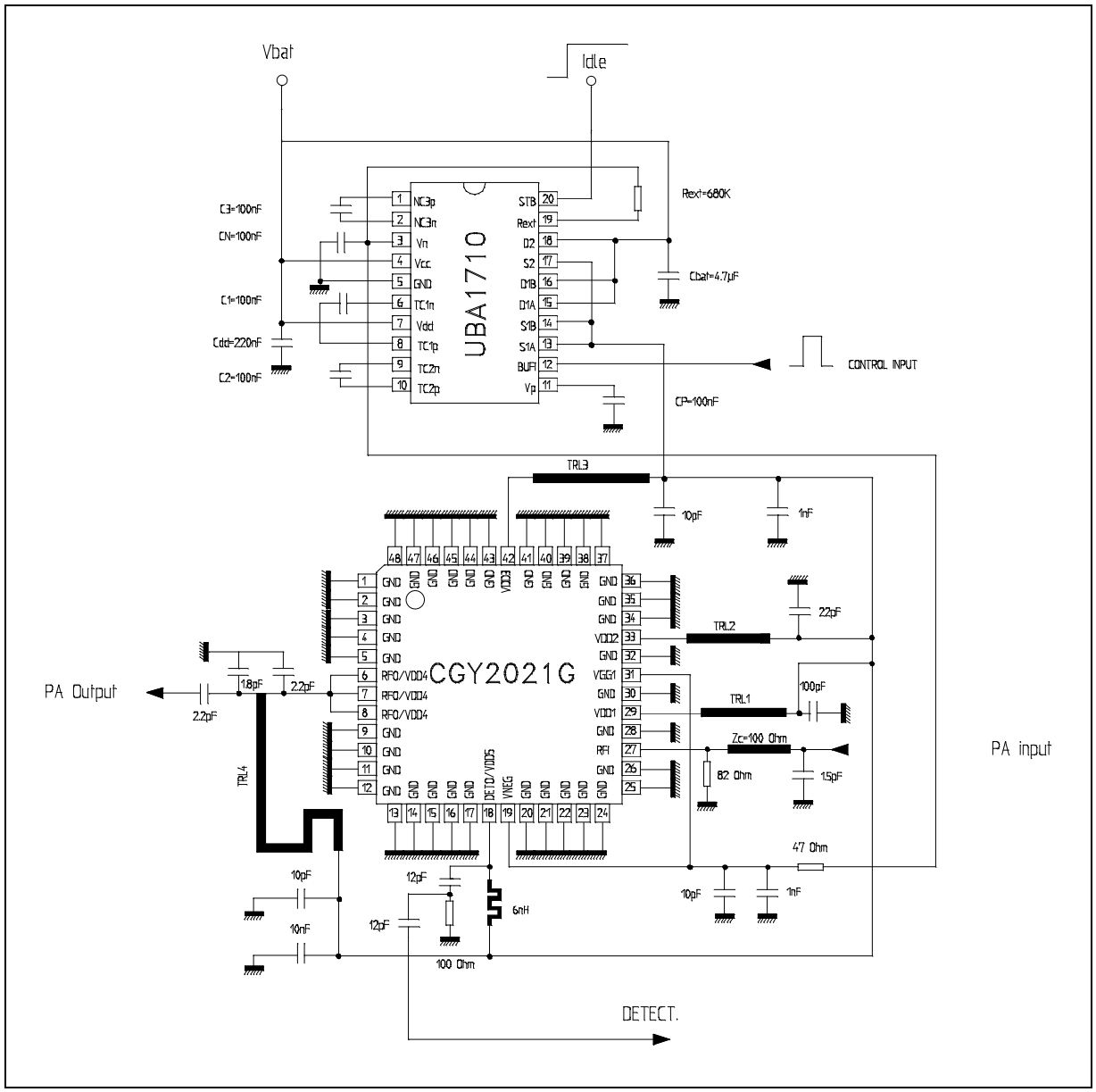

Fig. 6 Circuit diagram

6.2 Recommendations for use

6.2.1 Without UBA1710

As the device makes use of the normally on MESFET technology , a negative biasing applied to the gates must be set prior the drain voltage in order to avoid any power dissipation exess .

6.2.2 With UBA1710

When used with a power modulator (UBA1710) no particular precaution is necessary as long as the power amplifier is connected to the UBA1710 .

The power modulator has a built in power management that disables the drain voltage as long as the negative bias applied to the gates is higher than -1V .

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout making use of a CGY2021G and a UBA1710 is given in fig. 7 .
The characteristics of the substrate in use for the PCB are as following:
-substrate type:FR4 double clad
-Relative permetivity:εr=4.7
-Thickness:H=0.8mm
-Size:35x42mm

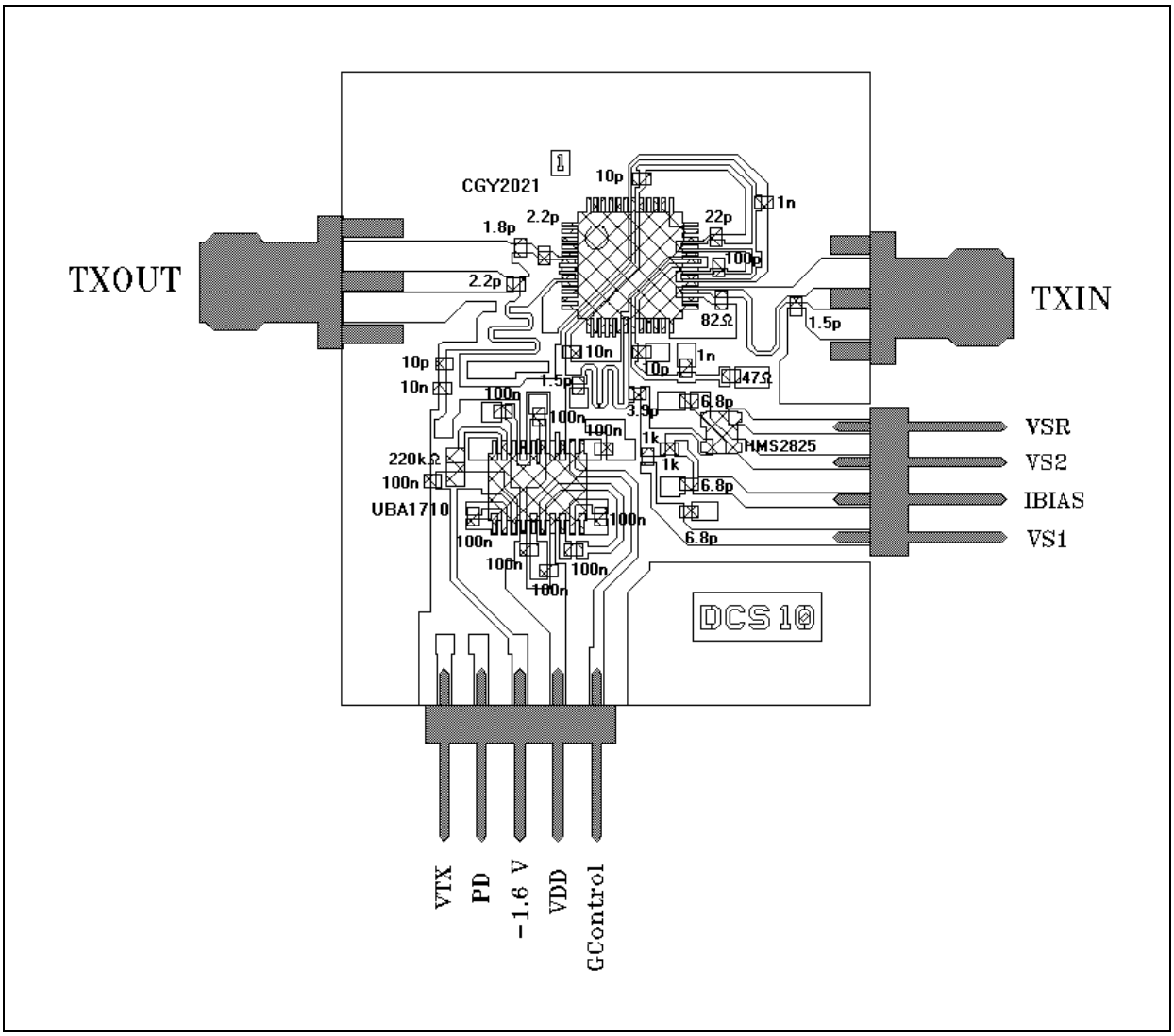

Fig. 7 Circuit layout

7.2 Part list DCS power amplifier with UBA1710

CAPACITORS (Size:0603)	
VALUE	**NUMBER**
1.5 pF	2
1.8	1
2.2	2
3.9 pF	1
6.8 pF	3
10 pF	3
22 pF	1
100 pF	1
1 nF	2
10 nF	2
100 nF	9

RESISTORS (Size:0603)	
VALUE	**NUMBER**
47 Ω	1
82 Ω	1
1kΩ	2
220kΩ	1

ACTIVE COMPONENTS	
CGY2021G	1
UBA1710	1
HMS2825	1

8. THERMAL CHARACTERISTICS

8.1 Thermal Characteristics

The maximum average dissipation is 1.3 W for a channel temperature not exeeding Tch=150 °C .

The thermal impedance from channel to ambient is typically Rthjc=45 K/W .This impedance is measured under nominal DCS/PCS pulse conditions .

8.2 Power derating curve

For safety and reliability reasons a power derating curve relative to the power dissipation is introduced and given in Fig 8.

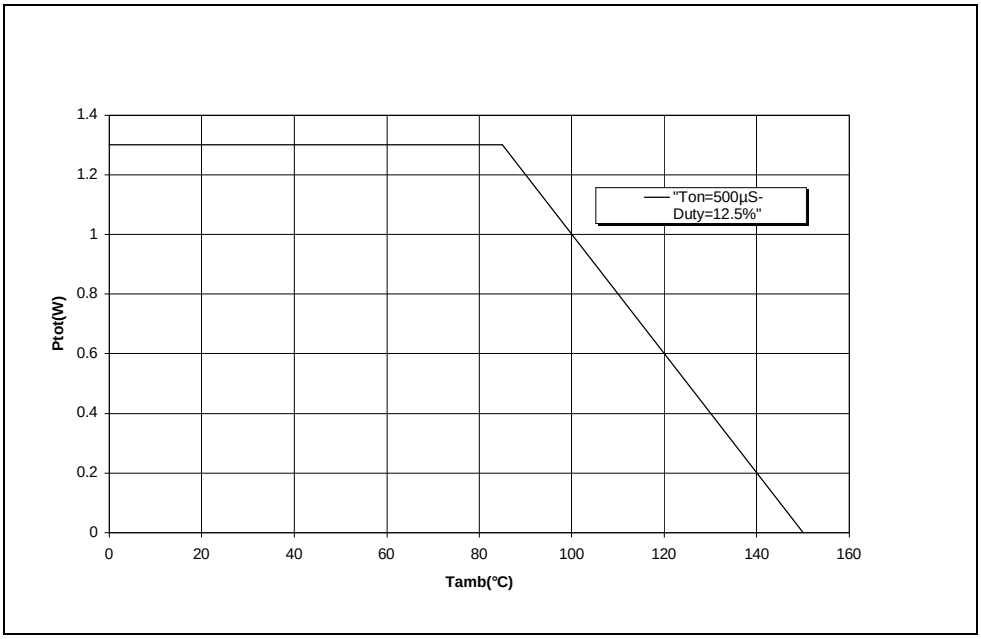

Fig. 8 Power derating

9. ELECTRICAL CHARACTERISTICS

9.1 Output power and efficiency as a function of drain voltage

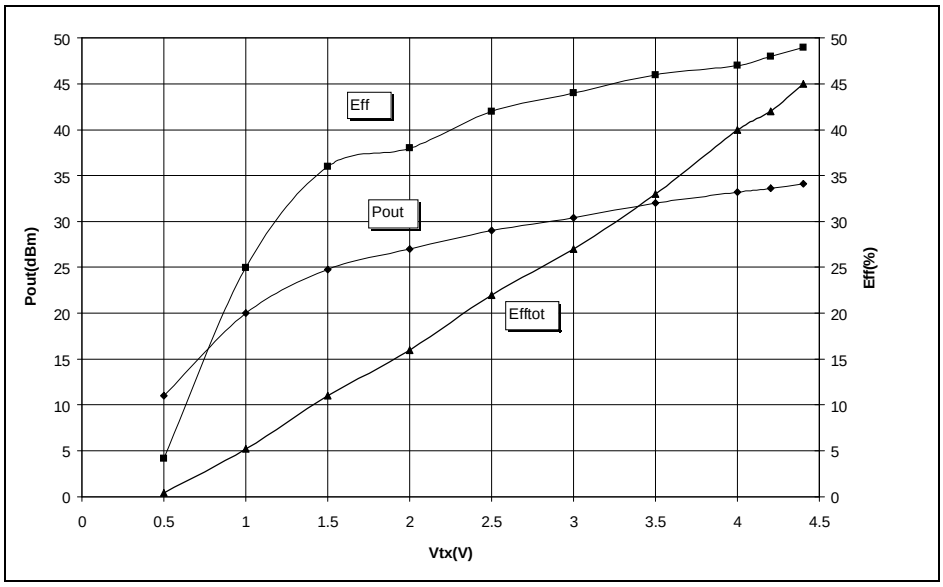

Fig. 9 Output power and efficiency versus drain voltage

9.2 Output power and return losses as a function of frequency

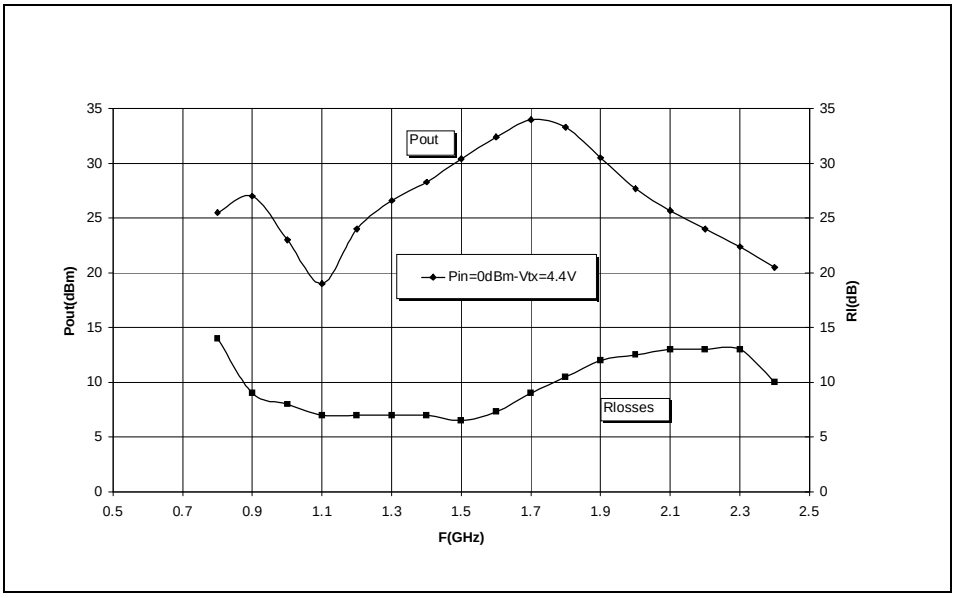

Fig. 10 Output power and input return losses versus frequency

9.3 Small signal gain and input/ouput return losses

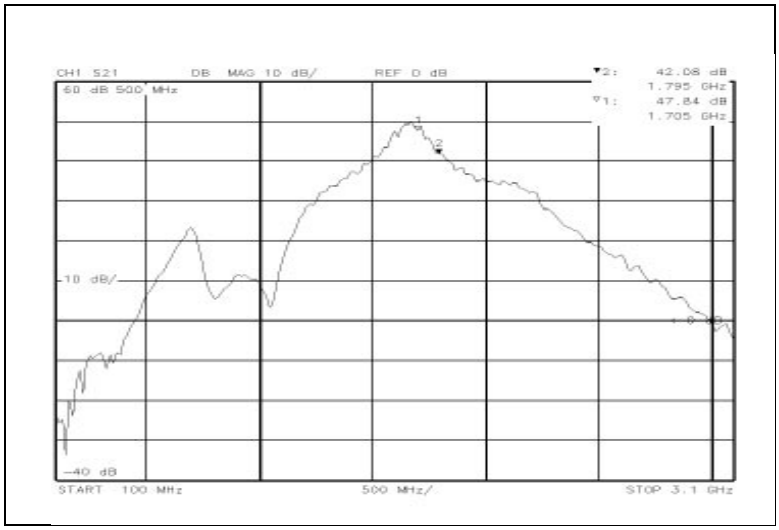

Fig. 11 Small signal gain versus frequency

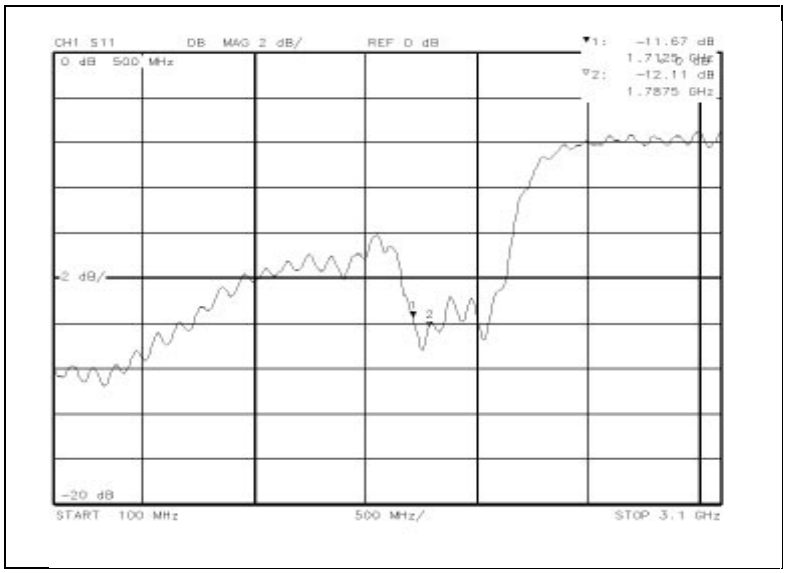

Fig. 12 Small signal input return losses

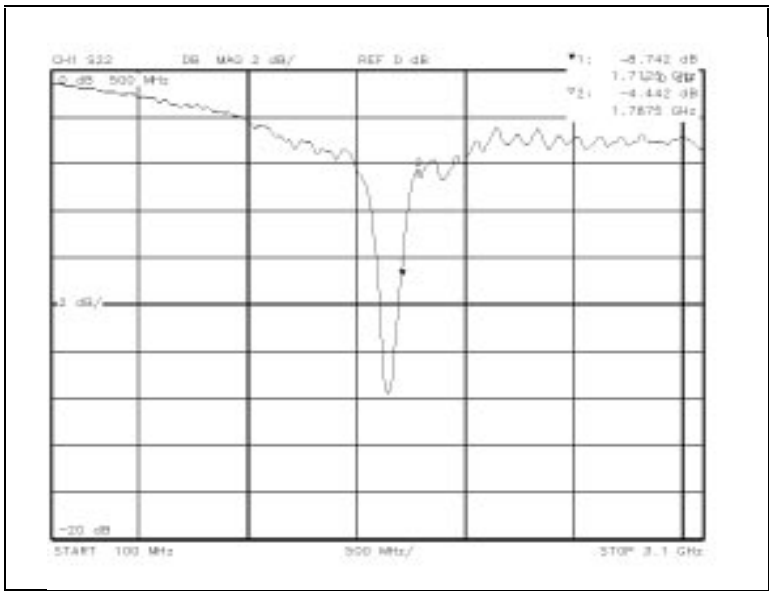

Fig. 13 Small signal output return losses

9.4 Output power as a function of input power

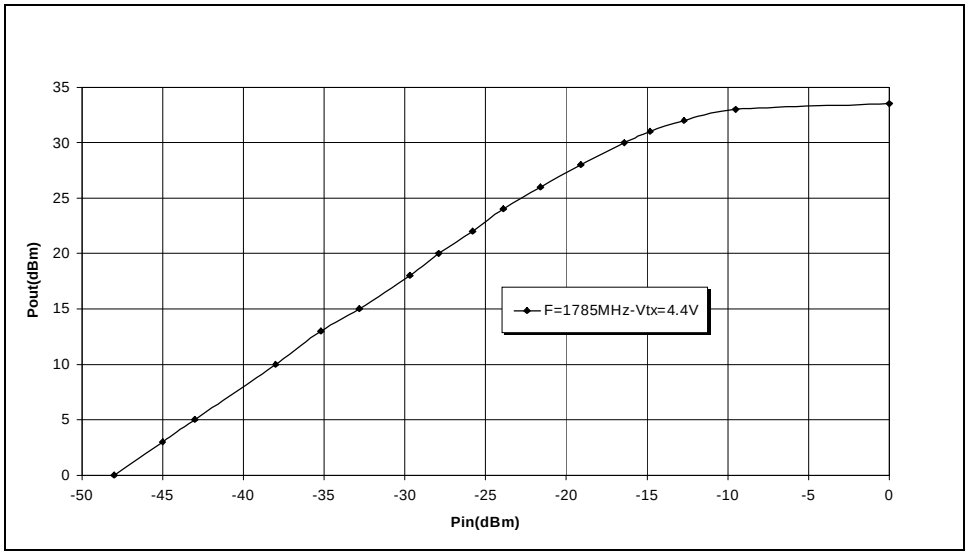

Fig. 14 Output power versus input power

9.5 Spurious gain as a function of frequency

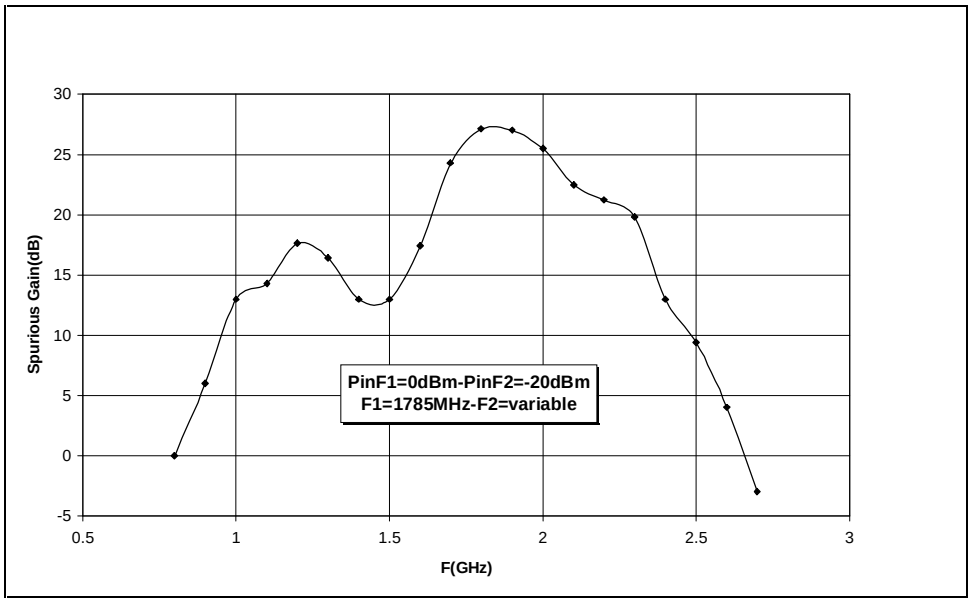

Fig. 15 Spurious gain versus frequency

9.6 Intermodulation gain as a function of output power

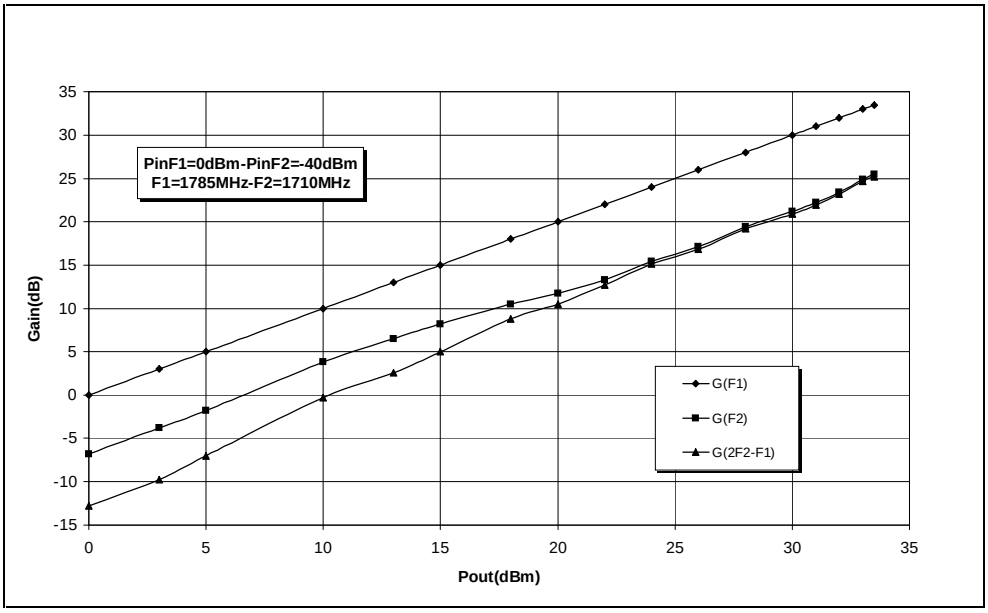

Fig. 16 Intermodulation gain versus output power

9.7 AM/PM conversion as a function of output power

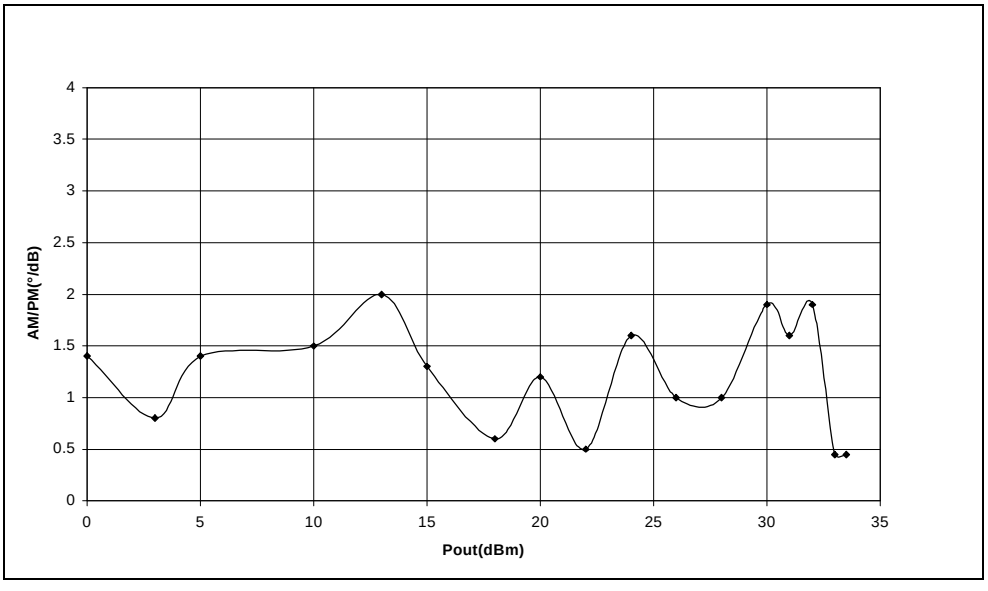

Fig. 17 AM/PM conversion versus output power

9.8 AM/AM conversion as a function of output power

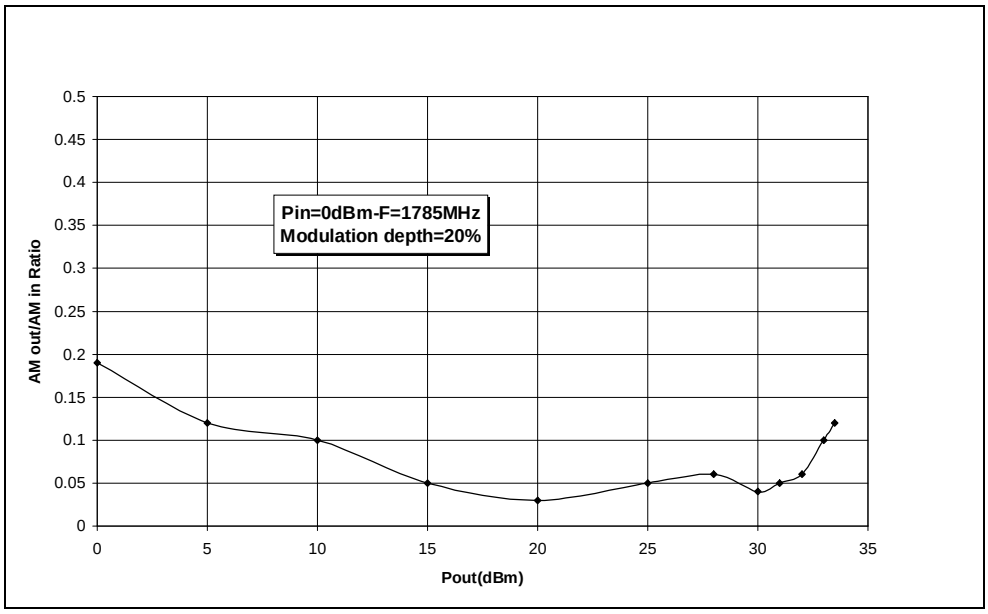

Fig. 18 AM/AM conversion versus output power

9.9 Noise conversion as a function of frequency

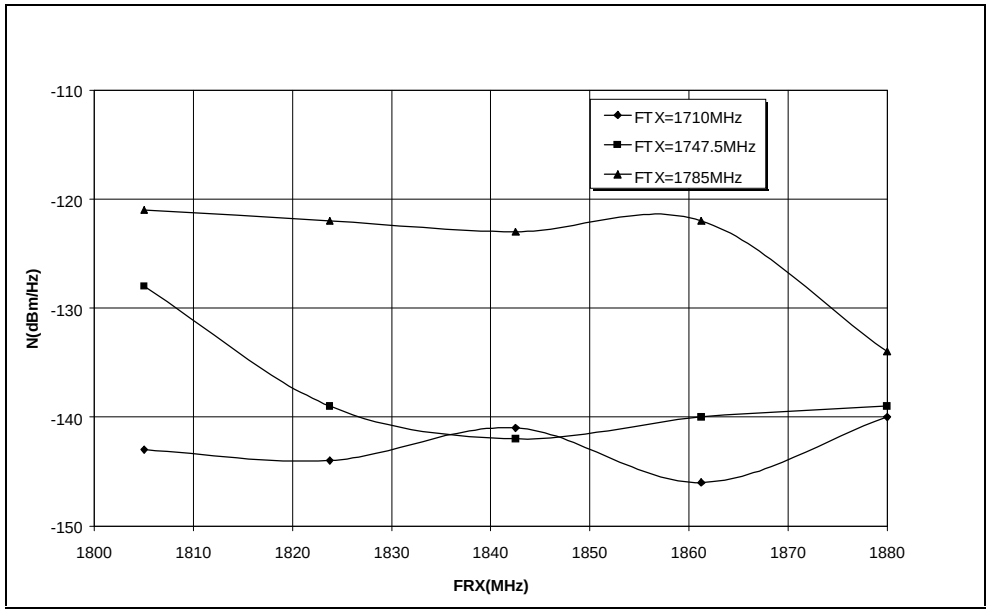

Fig. 19 Noise conversion versus frequency

9.10 Settling time in association with UBA1710

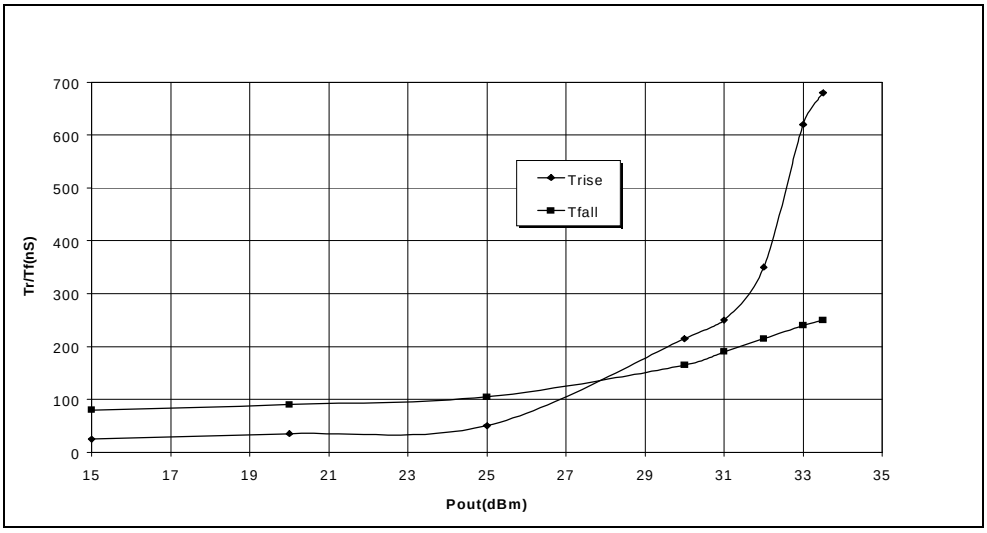

Fig. 20 Settling time versus output power

10. MODELIZATION AND SIMULATION

As the non linear models of the MESFET in use for the CGY2021G are known with a good accuracy , we can predict the dynamic performances of the power amplifier .

A relevant simulation concerning the output power and efficiencies versus the voltage exhibit a close correlation to the nominal measurements performed on the demoboard .See fig. 21
The CGY2021G models including the package parasitics are available on request for simulations and power amplifier designs in other frequency ranges like PCS for example .

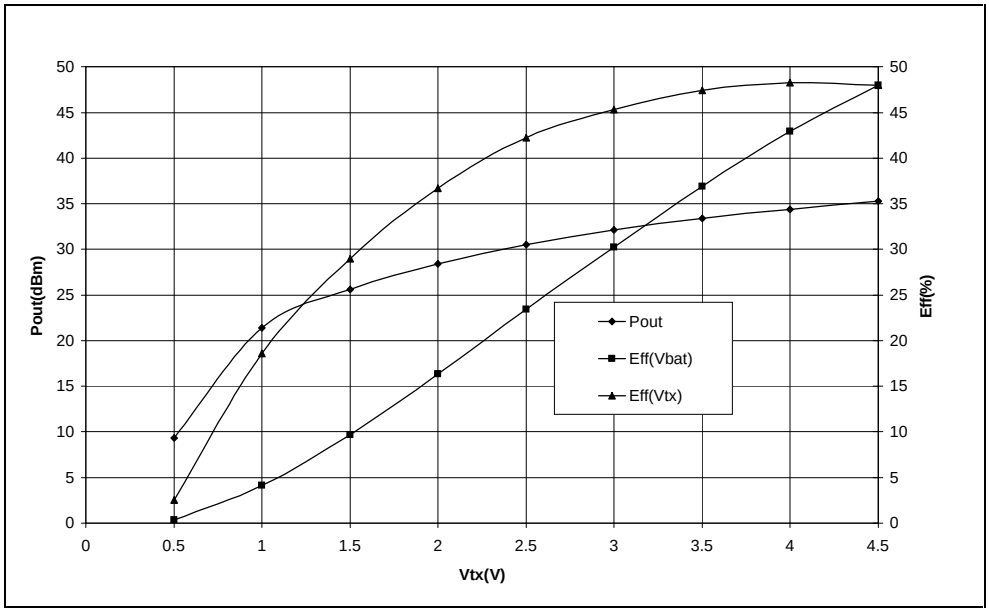

Fig. 21 Power control simulation